REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested.

Claim Objections

Defects in claims 1-2, and 5-7 have been corrected by the foregoing amendments. Specifically, claims 2 and 5 have been amended to provide antecedent basis for the "external signal lines" in claim 2 and "bit line" in claim 5.

The Office Action objected to the absence of the "6T memory cell" in the drawings. It is noted that in the background of the invention, conventional 6-transistor (6T) SRAM cells are discussed. The term "6T memory cell" refers to a cell having 6 transistors, as is well known in the art. There are two such 6T cells in each of FIGs 2, 3: P1-4, N1-2, and P11-14, N11-12 in FIG. 2; and P21-22, N21-24, and P31-32, N31-34 in FIG. 3. Unlike FIG. 1, FIGs. 2, and 3 illustrate full CAM cells, i.e. two half CAM cells. Each half CAM cell includes a 6T ternary memory cell, and a pair of transistors for comparison of search and stored data as is described on page 2 lines 1-3.

Claim 1 has been amended to provide antecedent basis for the half CAM cell, and to indicate that it is the half of the CAM cell that is qualified by the claim body, as opposed to half of the 6T ternary memory cells. The illustrated 6T ternary memory cells are not characterized by an equal number of p-type and n-type transistors.

Applicants submit that an equal number of transistors of the respective types is a clear definition of the invention, and this is supported in the description. Applicants further submit that the specific number of transistors in the illustrated embodiments is not intended to be limiting to the scope of the invention, but that the parity of n-type and p-type transistors permits the compact arrangement of the CAM cells.

Applicants have amended claim 6 to claim that the conductive layers includes at least one polysilicon layer, "conductive layers" being introduced in claim 1, lines 7 and 9.

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Claim 7 has also been amended to distinguish between the CAM cells and 6T memory cells.

It is respectfully submitted that the claims as amended are clear and supported by the specification. The claim objections are thereby traversed.

Claim Rejections 35 U.S.C. § 102

Claims 1-7 stand rejected as anticipated by Calin et al. USP 6,195,278. The Office Action states that each half cell of FIG. 2B has an equal number of transistors of n- and p-types. With respect, Applicants disagree. As defined by Calin et al. (col. 5, lines 16-20), in the embodiments of FIGs. 2A,2B "The CAM cells each comprise a standard six transistor SRAM cell 80, along with two p-channel pass transistors 82a, 82b, and an n-channel chain transistor 84." There are 9 transistors in the illustrated embodiment: 4 p-type transistors and 5 n-type transistors.

Accordingly, Applicants submit that Calin et al. do not anticipate the claimed invention of any of claims 1-7 which all claim that an equal number of n-type and p-type transistors are included in each half of the CAM cell.

For the reasons set forth above in detail, it is respectfully submitted that each of the claims 1-7 pending in this application are now in a condition for immediate allowance. Favorable reconsideration and early issuance of a Notice of Allowance are therefore requested.

Respectfully submitted,
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